AMENDMENTS TO THE CLAIMS

This listing of claims will replace all other versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A video controller for interfacing a frame buffer to a display in a computer system, comprising:

a raster engine adapted to receive video data from the frame buffer, to format the video data, and to render the formatted data to the display; and

a hardware blink logic system operatively associated with the raster engine to selectively blink at least one pixel on the display;

wherein formatting the video data comprises selectively remapping the video data to a format appropriate for interfacing with a selected one of a plurality of display device types.

2. (Original) The video controller of claim 1, further comprising a blink mode control register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink mode, wherein the hardware blink logic system is adapted to selectively blink at least one pixel on the display according to the selected blink mode.

3. (Original) The video controller of claim 2, wherein the selected blink mode comprises one of pixels ANDed with blink mask, pixels ORed with blink mask, pixels XORed with blink mask, blink to background, blink to offset color single value mode, blink to offset color 888 mode, blink dimmer, blink brighter, blink dimmer 888 mode, blink brighter 888 mode, and blink mode disabled.

4. (Original) The video controller of claim 3, wherein the hardware blink logic system is adapted to identify at least one blinking pixel according to the formatted data, and to

PAGE 2/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16

selectively blink the at least one blinking pixel on the display according to the selected blink mode.

5. (Original) The video controller of claim 2, wherein the hardware blink logic system is adapted to identify at least one blinking pixel according to the formatted data, and to selectively blink the at least one blinking pixel on the display according to the selected blink mode.

6. (Original) The video controller of claim 5, further comprising a blink mask control register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink mask, wherein the selected blink mode comprises one of pixels ANDed with blink mask, pixels ORed with blink mask, and pixels XORed with blink mask, and wherein the hardware blink logic system is adapted to selectively blink the at least one blinking pixel on the display according to the selected blink mode and the selected blink mask.

7. (Original) The video controller of claim 6, further comprising a blink rate register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink rate, wherein the hardware blink logic system is adapted to selectively blink the at least one blinking pixel on the display according to the selected blink mode, the selected blink mask, and the selected blink rate.

8. (Original) The video controller of claim 6, wherein the selected blink mode comprises pixels ANDed with blink mask, and wherein the hardware blink logic system is adapted to perform a logical AND operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

9. (Original) The video controller of claim 6, wherein the selected blink mode comprises pixels ORed with blink mask, and wherein the hardware blink logic system is adapted to perform a logical OR operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

PAGE 3/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16

10. (Original) The video controller of claim 6, wherein the selected blink mode comprises pixels XORed with blink mask, and wherein the hardware blink logic system is adapted to perform a logical exclusive OR operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

11. (Original) The video controller of claim 5, wherein the selected blink mode comprises one of blink to background, blink to offset color single value mode, blink to offset color 888 mode, blink dimmer, blink brighter, blink dimmer 888 mode, and blink brighter 888 mode, and wherein the hardware blink logic system is adapted to selectively blink the at least one blinking pixel on the display according to the selected blink mode and the selected blink mask.

12. (Original) The video controller of claim 11, further comprising a blink offset register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink offset, wherein the selected blink mode comprises one of blink to background, blink to offset color single value mode, and blink to offset color 888 mode, and wherein the hardware blink system is adapted to selectively replace formatted data associated with the at least one blinking pixel with the selected blink offset.

13. (Original) The video controller of claim 11, wherein the selected blink mode comprises one of blink dimmer, blink brighter, blink dimmer 888 mode, and blink brighter 888 mode, and wherein the hardware blink system is adapted to selectively shift bits of formatted data associated with the at least one blinking pixel.

14. (Original) The video controller of claim 11, further comprising a blink rate register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink rate, wherein the hardware blink logic system is adapted to selectively blink the at least one blinking pixel on the display according to the selected blink mode, the selected blink mask, and the selected blink rate.

PAGE 4/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16

15. (Previously Presented) In a video controller, a method of interfacing a frame buffer to a display in a computer system, comprising:

providing a raster engine adapted to receive video data from the frame buffer, to format and selectively remap the video data, and to render the formatted and selectively remapped data to the display; and

selectively blinking at least one pixel on the display using a hardware blink logic system operatively associated with the raster engine.

16. (Original) The method of claim 15, wherein the video controller comprises a blink mode control register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink mode, further comprising selectively blinking at least one pixel on the display according to the selected blink mode using the hardware blink logic system.

17. (Original) The method of claim 15, wherein the selected blink mode comprises one of pixels ANDed with blink mask, pixels ORed with blink mask, pixels XORed with blink mask, blink to background, blink to offset color single value mode, blink to offset color 888 mode, blink dimmer, blink brighter, blink dimmer 888 mode, blink brighter 888 mode, and blink mode disabled.

18. (Original) The method of claim 17, further comprising:

identifying at least one blinking pixel according to the formatted data using the hardware blink logic system; and

selectively blinking the at least one blinking pixel on the display according to the selected blink mode using the hardware blink logic system.

19. (Original) The method of claim 16, further comprising:

identifying at least one blinking pixel according to the formatted data using the hardware blink logic system; and

selectively blinking the at least one blinking pixel on the display according to the selected blink mode using the hardware blink logic system.

PAGE 5/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16

20. (Original) The method of claim 19, wherein the video controller comprises a blink mask control register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink mask, wherein the selected blink mode comprises one of pixels ANDed with blink mask, pixels ORed with blink mask, and pixels XORed with blink mask, further comprising selectively blinking the at least one blinking pixel on the display according to the selected blink mode and the selected blink mask using the hardware blink logic system.

21. (Original) The method of claim 20, wherein the video controller comprises a blink rate register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink rate, further comprising selectively blinking the at least one blinking pixel on the display according to the selected blink mode, the selected blink mask, and the selected blink rate using the hardware blink logic system.

22. (Original) The method of claim 20, wherein the selected blink mode comprises pixels ANDed with blink mask, further comprising performing a logical AND operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

23. (Original) The method of claim 20, wherein the selected blink mode comprises pixels ORed with blink mask, further comprising performing a logical OR operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

24. (Original) The method of claim 20, wherein the selected blink mode comprises pixels XORed with blink mask, further comprising performing a logical exclusive OR operation on formatted data associated with the at least one blinking pixel using the selected blink mask.

25. (Original) The method of claim 19, wherein the selected blink mode comprises one of blink to background, blink to offset color single value mode, blink to offset color 888 mode, blink dimmer, blink brighter, blink dimmer 888 mode, and blink brighter 888 mode, further

PAGE 6/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16

comprising selectively blinking the at least one blinking pixel on the display according to the selected blink mode and the selected blink mask using the hardware blink logic system .

26. (Original) The method of claim 25, wherein the video controller comprises a blink offset register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink offset, and wherein the selected blink mode comprises one of blink to background, blink to offset color single value mode, and blink to offset color 888 mode, further comprising selectively replacing formatted data associated with the at least one blinking pixel with the selected blink offset using the hardware blink system.

27. (Original) The method of claim 25, wherein the selected blink mode comprises one of blink dimmer, blink brighter, blink dimmer 888 mode, and blink brighter 888 mode, further comprising selectively shifting bits of formatted data associated with the at least one blinking pixel using the hardware blink system.

28. (Original) The method of claim 25, wherein the video controller comprises a blink rate register operatively associated with the hardware blink logic system and programmable via the computer system to select a blink rate, further comprising selectively blinking the at least one blinking pixel on the display according to the selected blink mode, the selected blink mask, and the selected blink rate using the hardware blink logic system.

29. (Currently Amended) A video controller for interfacing a frame buffer to a display in a computer system, comprising:

a raster engine adapted to receive video data from the frame buffer, to format and selectively remap the video data, and to render the formatted and selectively remapped data to the display; and

means for selectively blinking at least one pixel on the display operatively associated with the raster engine.

PAGE 7/10 * RCVD AT 3/21/2005 4:59:37 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:216 696 8731 * DURATION (mm-ss):03-16